Amendments to the Claims:

Please cancel claims 11 - 17 and 20 without prejudice or disclaimer of the subject matter thereof noting that claims 18 and 19 and previous original claims have been previous canceled and add the following new claims.

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-10 (Cancelled)

Claims 11 - 17 (canceled)

Claims 18 and 19 (canceled)

Claim 20 (canceled)

21. (new) A semiconductor processing apparatus, comprising:

a chamber in which a sample wafer as a processing object is processed;

first and second data storing devices each receiving and storing process data from the chamber which is generated during processing of at least the sample wafer, the process data including data concerning emission light generated within the chamber during the processing; and

a selecting device which selectively sends the process data to one of the first and second data storing devices in accordance with a predetermined condition;

wherein the selecting device sends the process data to one of the first and second data storing devices until an amount of the process data which has been sent to and stored in the one of the first and second data storing devices reaches a

predetermined amount as the predetermined condition, and thereafter sends the process data of a succeeding process to the other of the first and second data storing devices.

22. (new) A semiconductor processing apparatus according to claim 21, wherein the selecting device which selectively sends the process data to one of the first and second data storing devices in accordance with an amount of the process data having been sent to and stored in the first data storing device or the second data storing device.

23. (new) A semiconductor processing apparatus according to claim 21, wherein the selecting device sends the process data to one of the first and second data storing devices until the process data of one of (a) a predetermined date and a time period, (b) a predetermined time period, and (c) a predetermined at least one lot, has been sent to and stored in the one of the first and second data storing devices, and thereafter sends the process data of a succeeding process to the other of the first and second data storing devices.

24. (new) A semiconductor processing apparatus according to claim 21, wherein one of the first data storing device and the second data storing device is configured so as to be detachable from the semiconductor processing apparatus.

25. (new) A semiconductor processing apparatus according to claim 21, wherein the second data storing device is configured so as to be able to read the process data stored therein which is to be analyzed while the first data storing device

stores the process data from the chamber which is generated during processing of the at least the sample wafer which is to be analyzed.

26. (new) A semiconductor processing apparatus according to claim 22, wherein one of the first data storing device and the second data storing device is configured so as to be detachable from the semiconductor processing apparatus.

27. (new) A semiconductor processing apparatus according to claim 22, wherein the second data storing device is configured so as to be able to read the process data stored therein which is to be analyzed while the first data storing device stores the process data which is to be analyzed from the chamber and which is generated during processing of the at least the sample wafer.

28. (new) A semiconductor processing apparatus according to claim 27, wherein one of the first data storing device and the second data storing device is coupled to a different path through which the process data stored in one of the first data storing device and the second data storing device is read, the different path being different from a path through which the process data is sent to the one of the first data storing device and the second data storing device.

29. (new) A semiconductor processing apparatus according to claim 28, further comprising a data analyzer which analyzes the process data stored in one of the first data storing device and the second data storing device and read via the different path, whereby the processing of the wafer is adjusted in accordance with a result of the analysis of the data analyzer.

30. (new) A semiconductor processing apparatus according to claim 27, further comprising a data analyzer which analyzes the process data stored in one of the first data storing device or the second data storing device, whereby the processing of the wafer is adjusted in accordance with a result of the analysis of the data analyzer.

31. (new) A semiconductor processing apparatus according to claim 23, wherein one of the first data storing device and the second data storing device is configured so as to be detachable from the semiconductor processing apparatus.

32. (new) A semiconductor processing apparatus according to claim 23, wherein the second data storing device is configured so as to be able to read the process data stored therein which is to be analyzed while the first data storing device stores the process data which is to be analyzed from the chamber and which is generated during processing of the at least the sample wafer.

33. (new) A semiconductor processing apparatus according to claim 32, wherein one of the first data storing device and the second data storing device is coupled to a different path through which the process data stored in one of the first storing device and the second data storing device is read, the different path being different from a path through which the process data is sent to the one of the first data storing device and the second data storing device.

34. (new) A semiconductor processing apparatus according to claim 33, further comprising a data analyzer which analyzes the process data stored in one of the first data storing device and the second data storing device and read via the different path, whereby the processing of the wafer is adjusted in accordance with a result of the analysis of the data analyzer.

35. (new) A semiconductor processing apparatus according to claim 32, further comprising a data analyzer which analyzes the process data stored in one of the first data storing device or the second data storing device, whereby the processing of the wafer is adjusted in accordance with a result of the analysis of the data analyzer.

36. (new) A semiconductor processing apparatus according to claim 25, wherein one of the first data storing device and the second data storing device is coupled to a different path through which the process data stored in one of the first storing device and the second data storing device is read, the different path being different from a path through which the process data is sent the one of to the first data storing device and the second data storing device.

37. (new) A semiconductor processing apparatus according to claim 25, further comprising a data analyzer which analyzes the process data stored in one of the first data storing device and the second data storing device, whereby the processing of the wafer is adjusted in accordance with a result of the analysis of the data analyzer.

38. (new) A semiconductor processing apparatus according to claim 36, further comprising a data analyzer which analyzes the process data stored in one of the first data storing device and the second data storing device and read via the different path, whereby the processing of the wafer is adjusted in accordance with a result of the analysis of the data analyzer.